

APPENDIX D

**(VERSION OF CLAIMS AS AMENDED HEREIN
WITH MARKINGS TO SHOW CHANGES MADE)**

(Serial No. 09/943,778)

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

9. (Amended) The DRAM circuit of claim [1]2, wherein said TEOS layer comprises a dopant barrier between said capacitor structure and said insulating layer.

10. (Amended) A semiconductor memory device comprising:
a semiconductor substrate having a capacitor structure formed thereon, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer[,] and said first and second conductive layers having an end portion;
a conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer; and
a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer,
said TEOS layer disposed between said capacitor structure and said conductive contact.

20. (Amended) The device of claim [10]11, wherein said TEOS layer comprises a dopant barrier between said capacitor structure and said insulating layer.